Breakthroughs in Analog and RF Circuit Performance through Steep-Slope FinFETs

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Abstract— Fin-shaped Field-Effect Transistors (FinFETs) with Three Independent Gates (TIG) have been recently demonstrated capable of an ultra-steep-slope operation down to 3.4mV/dec. In this paper, we explore their opportunities in the domain of analog design and terahertz detectors. We see that they could result in analog circuits with $25 \times$ power efficiency improvement and in THz detectors with 2 orders of magnitude higher sensitivity.

I. INTRODUCTION

In order to sustain the ever-increasing need for computing performance, the semiconductor industry introduced many device-level innovations during the last decade. On the one hand, novel device geometries, such as FinFETs [1], or FDSOI [2], have been successfully employed to improve the current density, reduce the leakage floor and reduce the short-channel effects at advanced technology nodes. On the other hand, complex materials, such as high-K gate stacks, silicon-germanium channels or copper-based interconnects were additionally leveraged to allow the device scalability down to the contemporary 14nm technology node. However, the basic operation principle, i.e., thermionic emission, remains unchanged since the introduction of MOSFETs. Unfortunately, this imposes a physical limitation on the minimum Subthreshold Slope (SS) achievable by conventional MOSFETs and subsequently sets an upper bound on the level of performances reachable by many analog and RF circuits [3].

In parallel to the focus on scaling, an interesting approach consists in increasing the functionalities of the basic transistors by means of additional gate [4]–[7]. In particular, a FinFET device exploiting silicided contacts and additional gate contacts to bias the Schottky barriers has been recently shown capable of a minimal subthreshold slope of 3.4mV/dec and an average subthreshold slope of 6mV/dec over 5 decades of current [7]. The efficiency of this device to break the fundamental limit of the SS in conventional MOSFETs open many opportunities to create analog systems with capabilities unattainable with current technologies.

In this paper, we make the link between the capabilities of steep-slope FinFET devices and the challenges of analog and RF design. In particular, we see that the propose device could result in a massive $25 \times$ power efficiency improvement for a wide range of analog circuits and that THz detectors can be designed with room-temperature current-responsivities in the order of 2 orders of magnitude larger than with conventional technologies.

II. ULTRA-STEEP-SLOPE FINFETS

A conceptual structure of the steep-slope FinFET device is depicted in Fig. 1-a. The device exploits fin-based channel with metallic Source (S) and Drain (D) contacts. The Schottky-Bias (SB) terminal electrostatically modulates the barrier heights at S/D. The Gate (G) terminal acts conventionally, by creating a potential barrier in the channel and turning the device on or off.

The proposed device is fabricated with a dopant-free process on an SOI wafer, where 340nm-high and 40nm-thick fins are patterned [7]. Subsequently to the active region patterning
and a 15nm-thick gate dielectric formation, three 200nm-long gate terminals are realized by self-alignment. Nickel silicide is used to form near-midgap Schottky-barriers at S/D. Note that the large dimensions of the device are used to mitigate the variability of an academic cleanroom environment and no physical limitations precludes the use of more aggressive dimensions. The resulting fabricated device is shown in Fig. 1-b.

The operation of the device is illustrated in Fig. 2-a. The application of a positive bias potential $V_{SB}$ creates a potential well under the gate and is key to obtain a steep-slope behavior as shown in [7]. When electrons acquire enough energy, weak impact ionization is triggered and electron/hole pairs are generated (step 1). The generated holes accumulate in the potential well under the gate (step 2). This lowers the barrier and provides more electrons for impact ionization, thus establishing a positive feedback. During the transition, the energy band in the SB region is lowered (step 3), maintaining the potential well for the accumulation and improving the average SS over the subthreshold region. While Fig. 2-a represents an $n$-type configuration, $p$-type configuration can be achieved by applying a negative $V_{SB}$ potential [7].

Fig. 2-b shows the characteristics of the fabricated steep-slope FinFET, carried out at room temperature [7]. Minimum SS of 3.4 mV/dec is achieved. An average SS of 6.0 mV/dec is observed for 5 decades of current. When decreasing $V_{DS}$, the impact ionization rate decreases, and the SS gradually degrades to 61 mV/dec at $V_{DS} = 1V$. Complete $n$-type and $p$-type characteristics are available in [7].

### III. HIGH-PERFORMANCE ANALOG DESIGN OPPORTUNITIES

In this section, we explore the opportunities offered by the novel steep-slope FinFET in the design of analog and RF circuits.

#### A. Analog Circuit Design

Analog circuit performance is fundamentally linked to transistor figures of merit including transconductance efficiency ($g_{m}/I_D$), transit frequency ($g_{m}/C_{gs}$), and intrinsic gain ($g_{m}/g_{ds}$) [3], [8], [9]. These metrics dictate constraints in the power consumption, speed, and gain of analog circuits. Power efficiency, for instance, involves a tradeoff between the bias current required to achieve a certain transconductance ($g_{m}/I_D$), and the resulting device capacitance that contributes to circuit loading ($g_{m}/C_{gs}$). For CMOS transistors operating in weak inversion, $g_{m}/I_D$ is directly coupled to Subthreshold Slope (SS) by:

$$\frac{g_{m}}{I_D} = 1 \frac{\partial I_D}{\partial V_g} = \frac{\partial (\ln(I_d))}{\partial V_g} = \frac{\ln(10)}{SS}$$

This limit results from the physics of thermionic emission and gate control of surface potential. With perfect surface potential control, a MOSFET could achieve $g_{m}/I_D \leq 40$ S/A (SS $\geq 60$mV/decade), but this is not practical due to finite depletion capacitance. Transistor scaling has led us to very fast transistors (high $g_{m}/C_{gs}$), resulting in more and more analog designs being pushed toward subthreshold operation in order to leverage the enhanced power efficiency (high $g_{m}/I_D$).

Measurements of Fig. 2-b show SS as steep as 3.4mV/dec, giving the potential for $g_{m}/I_D = 677$ S/A, which could result in a 25× power efficiency improvement for a wide range of analog circuits. A compelling, ubiquitous application is to replace the input pair of a CMOS differential amplifier with steep-slope TIGFETs. However, several challenges still have to be overcome before reaching such a level of performance. Indeed, a circuit challenge is to reliably bias the TIGFETs in the steep slope region, which can be achieved through replica biasing techniques and tight control of $V_{DS}$ through active cascode structures. Other challenges to be addressed through a combination of device and circuit engineering include noise, capacitance, finite $g_{ds}$, and reducing the required $V_{DS}$ required to achieve steep SS.

#### B. Terahertz Detectors

Many THz detection approaches have been developed to-date [10]. However, a miniaturized room-temperature detector
technology, exhibiting a very sensitive THz response, is still largely missing.

For instance, bolometric systems can display excellent noise equivalent powers (NEP \( \sim 10^{-14} W/Hz^{0.5} \)), but at the expenses of deep cryogenic operation and often a low dynamic range [11]. On the other hand, high-temperature THz detectors are either not very sensitive, or are extremely slow. Microbolometer THz focal plane arrays presently provide only moderate sensitivities (\( \sim 10^{-12} W/Hz^{0.5} \)) and response speed [12], [13]. Recent advances in electron devices have been opening a path for a new generation of THz detector technologies. Novel ultrafast electronic devices, such as heterostructure backward diodes can exhibit extremely high cutoff frequencies [14], and FETs have been demonstrated capable of operating at frequencies well above their cut-off frequency, e.g., [15]. Monolithically integrated backward diode THz detectors have been demonstrated showing a broadband response and NEP in the order of \( 8.5 \times 10^{-10} W/Hz^{0.5} \) [16]. Moreover, recent work on MOSFET THz detectors (as well as Schottky diode THz detectors) has shown NEP levels in the order of \( 10^{-10} \) to \( 10^{-12} W/Hz^{0.5} \) [17]–[20]. The overall panorama of THz detectors reported to-date is represented in Fig. 3.

Conventional MOSFETs can operate as efficient THz detectors far beyond their fundamental cut-off frequency [21]. Indeed, FETs can operate as non-resonant broadband THz detectors with high responsivity, as described by the Dyakonov-Shur theory. When a THz field is applied between the gate and the source terminal of the transistor, the THz electric field is rectified, like in square-law detectors, and a DC source-to-drain photo-voltage is induced. This voltage difference \( \Delta U \), called the detector photoresponse, can be expressed as a function of \( V_{GS} \) for a fixed drain bias by [22]:

\[
\Delta U = \frac{1}{4} \left[ \frac{1}{\sigma} \frac{d\sigma}{dU} \right]_{U=V_{GS}} = \frac{1}{4} \left[ \frac{d}{dV_{GS}} \ln [I_{DS}(V_{GS})] \right]
\]

(2)

Eq. (2) assumes conjugate matching of an antenna coupling the incoming THz radiation into the device and an infinite load impedance (from drain to source), i.e., \( Z_L = +\infty \). Therefore, it provides an upper bound for the device photoresponse. Thanks to this simple physical model, we can evaluate the potential of the TIGFETs for THz detection applications.

We estimate the maximum attainable current-responsivity \( R_i \) (\( R_i = \Delta U G_{DS}/P_{in} \)) where \( G_{DS} \) the drain-to-source conductance) from the measured device characteristics at room temperature (Fig. 2-b). The results of our calculations are depicted in Fig. 4. For the purpose of estimating the current-responsivity, the device \( I-V_{GS} \) characteristics were fitted to a model of the form given in [23].

It is observed that TIG FETs can achieve a much larger responsivity compared to a regular FET. While the maximum current-responsivity of regular thermally-limited FET detectors is in the order of \( R_i \approx 10 A/W \), TIGFETs can enable room-temperature current-responsivities up to 2 orders of magnitude larger, promising THz detectors with performances unachievable with regular FET (and also Schottky diode) technologies.

In order to estimate the Noise Equivalent Power (NEP) in TIGFET detectors, it is important to analyze the different sources of noise in such devices. Overall, the electrical noise can be divided into a thermal contribution and an excess part: \( S_V = S_{V,T} + S_{V,ex} \), where the excess part consists of: (a) 1/f^\alpha-type flicker noise (\( \alpha = 1 \)), and (b) generation-recombination-type noise, which varies as 1/f^2. There are essentially two physical mechanisms behind any fluctuations in electrical current: (1) fluctuations in the mobility, and (2) fluctuations in the number of carriers. In general, the excess noise can be attributed to carrier number fluctuations stemming from charge carrier capture, release and recombination events. In FinFETs as well as TIG FETs, the charge fluctuation in the gate dielectric could also induce fluctuations of the carrier mobility, giving rise to so-called Correlated Mobility Fluctuations (CMF). When analyzing all noise contributions,
it is found that 1/f noise mostly originates from the CMF due to trapping/de-trapping of channel carriers into slow gate dielectric traps [24], [25]. Our estimates for all the noise contributions in the TIGFET, under the bias conditions at which maximum responsivity is attained, show that generation-recombination and flicker noises dominate over thermal noise, as also observed by other authors [26], [27]. The total (current) noise spectral density is estimated to be on the order of $10^{-22} A^2/Hz$, which leads to projected NEP levels on the order of $10^{-14} W/Hz^{0.5}$, thus 2 orders of magnitude better performance than current room temperature THz detectors.

IV. CONCLUSION

In this paper, we evaluated the opportunities given by steep-slope FinFETs in the domain of analog design and terahertz detectors. We saw that they could result in a massive 25× power efficiency improvement for analog circuits and in 2 orders of magnitude more sensitive THz detectors.

REFERENCES